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EXAMINER	
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ART UNIT	PAPER NUMBER
2111	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/763,438	KONDO ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on th cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6 and 7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 8 and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 2-4, 6-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 2, it is unclear what may be "a destination module." Such a module and relationships thereof to other modules recited in claim 1 have not been clearly set forth.

With regard to claim 4, it is unclear what may be "a destination module." Such a module and relationships thereof to other modules recited in claim 1 have not been clearly set forth.

With regard to claim 6, it is unclear what may be "a destination module." Such a module and relationships thereof to other modules recited in claim 1 have not been clearly set forth. Also, it is unclear what may be "a source module." Such a module and relationships thereof to other modules recited in claim 1 have not been clearly set forth.

Further, the essential structural cooperative relationship(s) between the "means" and the "bus" and a plurality of modules have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

With regard to claim 7, it is unclear what may be "a destination module." Such a module and relationships thereof to other modules have not been clearly set forth.

With regard to claim 8, the essential structural cooperative relationship(s) between the "common buffer" and the "bus" and "plurality of functional modules" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

With regard to claim 9, "a first and a second bus" lacks clear antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartmann.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure that differs from Hartmann.

With regard to claims 1 and 8, Hartmann discloses an integrated circuit comprising: a plurality of functional modules (210 A-D comprising 220 A-D, for example); a bus (230A, for example) for interconnecting said plurality of functional modules; and a common buffer (a common buffer unit disposed inside 24 comprising input buffer 410A and output buffer 410B shared by 210A-D) disposed on said bus for storing transfer information transferred between any functional modules within said plurality of functional modules.

With regard to claim 2, it is clear that in Hartmann, the common buffer (discussed above) is set in a buffering enabled state (to store data) or a buffering disabled state (send data) depending
on whether or not a buffer (220) in a destination module can accept said transfer information (the module 210 signals a readiness to accept the data, see col. 5, lines 30-31. In another word, the buffer 220 of module 210 must be ready to accept data).

With regard to claim 3, the integrated circuit of Hartmann further comprising means for selecting a path (switching logic 430, for example) for transferring information to said destination module when a signal from said destination module indicates that the buffer within said destination module can accept information (see explanation regarding to claim 2 above), and selecting a transfer path for storing said transfer information in

said common buffer when the signal indicates that the buffer within said destination module cannot accept information (it is clear that when the module is not ready to accept data, the transfer information is stored in a common buffer unit disposed inside 24 comprising input buffer 410A and output buffer 410B shared by 210A-D, until the module is ready to accept data by signaling a readiness signal.

With regard to claim 4, the integrated circuit of Hartmann further comprising a signal line (260) for transferring said transfer information when a buffer within a destination module of said transfer information can accept a transfer (it is clear that buffer has to be ready before accepting data), said signal line circumventing said common 29 buffer (it is clear that the transfer information is not routed through the common buffer unit disposed inside 24 comprising input buffer 410A and output buffer 410B shared by 210A-D).

With regard to claim 5, the common buffer within said bus is located adjacent to each of said plurality of functional modules within said integrated circuit. Note that "adjacent" does not require absolute contact, but only requires relatively close position. Ex parte Hadsel (PO BdApp), 109 USPQ 509. Further, "adjacent" is broader than side by side. Ex parte Appeldorn & Gilkesen (PTO BdApp), 159 USPQ 791.

With regard to claim 7, see explanation regarding to claims 1, 3, and 4.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Qureshi et al. (Qureshi).

With regard to claims 1 and 8, Qureshi discloses an integrated circuit comprising: a plurality of functional modules (16, 18, 20, 22, 24, 40, 42, 44, and 46, for example); a bus (system bus 26) for interconnecting said plurality of functional modules; and a common buffer (VCI 73, see also Fig. 12 showing a block diagram of VCI) disposed on said bus for storing transfer information transferred between any functional modules within said plurality of functional modules.

With regard to claim 2, it is clear that in Qureshi, the common buffer (discussed above) is set in a buffering enabled state (to store data) or a buffering disabled state (send data) depending on whether or not a buffer (SVCI 30, for example) in a destination module can accept said transfer information (it is clear that data can only be sent from buffer VCI73 to buffer SVCI 30 when SVCI 30 is ready). In another word, the buffer SVCI30 must be ready to accept data).

With regard to claim 3, the integrated circuit of Qureshi further comprising means for selecting a path (in bridge 62) for transferring information to said destination module when a signal from said destination module indicates that the buffer within said destination module can accept information (see explanation regarding to claim 2 above), and selecting a transfer path for storing said transfer information in said common buffer when the signal indicates that the buffer within said destination module cannot accept information (it is clear that when the module is not ready to accept data, the transfer information is stored in a common buffer unit disposed inside VCI 73 until the module is ready to accept data.

With regard to claim 4, the integrated circuit of Qureshi further comprising a signal line (for connecting module 16 to 28, for example) for transferring said transfer information when a buffer within a destination module of said transfer information can accept a transfer (it is clear that buffer has to be ready before accepting data), said signal line circumventing said common buffer (it is clear that the transfer information is not routed through the common buffer VCI 73.

With regard to claim 5, the common buffer within said bus is located adjacent to each of said plurality of functional modules within said integrated circuit. Note that "adjacent" does not require absolute contact, but only requires relatively close position. Ex parte Hadsel (PO BdApp), 109 USPQ 509. Further, "adjacent" is broader than side by side. Ex parte Appeldorn & Gilkesen (PTO BdApp), 159 USPQ 791.

With regard to claim 6, the integrated circuit further comprising means (see at least claims 10-12, for example), operative when an information receiving buffer in a destination module cannot accept a transfer, for communicating information from said destination module to a source module, said information indicating that no transfer can be permitted.

With regard to claim 7, see explanation regarding to claims 1, 3, and 4.

With regard to claim 9, Qureshi discloses a integrated circuit comprising: a plurality of functional modules (16, 18, 20, 22, 24, 40, 42, 44, and 46, for example); and at least two on-chip buses (26 and 38) for interconnecting said plurality of functional modules, wherein a first bus and a second bus (26, 38) are interconnected through a bus adapter (62); and functional modules connected to said first bus (26) includes a

CPU module (18), an external memory interface module (16 for external memory), and said bus adapter (62).

With regard to claim 10, it is clear that the first bus and second buses are on-chip buses.

With regard to claim 11, it is clear that an operating frequency of said first bus (system bus 26) is an integer multiple of an operating frequency of said second bus (peripheral bus 38). As well-known in computer architecture, the system clock speed is different than peripheral clock speed. For example, a typical PCI bus is operated at 33 Mhz while an AGP is operated at 66 Mhz while the CPU is operated at a much higher frequency. In another word, an operating frequency of the system bus 26 is an integer multiple of an operating frequency of the peripheral bus 38.

Claims 1, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 1063616 (cited by Applicants).

To avoid repetition, Applicants' attention is directed to the detailed written opinion found in the Examination Report, which forms the basis of this rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not b negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hartmann in view of Qureshi.

Hartmann, as explained above, discloses the claimed invention. Hartmann does not disclose the use a "means, operative when an information receiving buffer in a destination module cannot accept a transfer, for communicating information from said destination module to a source module, said information indicating that no transfer can be permitted." Qureshi discloses the use of a means for indicating that no transfer can be permitted if the module cannot accept a transfer. See at least claims 10-12 of Qureshi. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Hartmann with a means for indicating that no transfer can be permitted if the module cannot accept a transfer, as taught by Qureshi, for the purpose of improving bus latency, for example.

U.S. Patent Nos. 6,597,692 to Venkitakrishnan, 6,111,859 to Godfrey et al., 6,601,126 to Zaidi et al., and 6,275,975 to Lambrecht et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner